IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

DeVries, et al.

Serial No.: S/N: 10/709,325 Group Art Unit: 2811

Filed: April 28, 2004 Examiner: Im, J. M.

For: **METHOD AND STRUCTURE FOR CONNECTING GROUND/POWER NETWORKS TO PREVENT CHARGE DAMAGE IN SILICON ON INSULATOR**

Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANTS' REPLY BRIEF ON APPEAL

Sir:

Appellants respectfully reply herein to the Examiner's Answer mailed on April 4, 2007, in the above-identified application.

Appellants respectfully submit that there are at least five fundamental flaws in the Examiner's position presented in the Examiner's Answer, as follows.

1. Even if all three references of record were to be combined, the combination would not result in the present invention described by the claims;

2. The Examiner's position fails to honor the terminology (e.g., "circuit design modules") used in the claims, as this terminology is defined in the specification;

3. The Examiner's position improperly ignores structural terminology (e.g., "grids of

circuit design modules" and "metallization layer") that is inherent in the claim language, even if the Examiner feels entitled to ignore "processing terminology";

4. The Examiner's position ignores the difference between the silicon-based technology of primary reference Liu and the SOI environment of the present invention and improperly attempts to convert the primary reference into the SOI environment that has a different breakdown mechanism; and

5. Because of the different breakdown mechanisms between bulk silicon and SOI, the protective mechanism in primary reference Liu (and secondary reference Finzi) fails to satisfy the plain meaning of the claim language of even the independent claims. Secondary reference Kimura does address the SOI environment but teaches a different concept to protect against damage during plasma processing.

1. Even if all three references of record were to be combined, the combination would not result in the present invention described by the claims

As explained in more detail below in (4), the mechanism of breakdown due to plasma processing is different in the bulk silicon environment of primary reference Liu and secondary reference Finzi than in the SOI environment of the present invention and secondary reference Kimura.

Essentially, the bulk silicon environment involves a path to the substrate and the protective devices in both Liu (see item 20 in Figure 2) and in Finzi (see item 220 in Figure 2, item 320 of Figure 3, and item 520 in Figure 5) involve an interconnection between a protected circuit point and the substrate. In these two bulk silicon examples, there is no suggestion to interconnect between two grids, let along the specific type of grid required in the independent claims (e.g., the grid of a circuit design module). Secondary reference Kimura does relate to breakdown during plasma processing in the SOI environment, but the solution in Kimura is to provide a protective dummy doped region if the ratio of wire area exceeds a threshold.

Therefore, none of three cited references, even if combined, provide a device having the structure defined in the independent claims. Kimura is the only one of the three that addresses the SOI environment, but its solution is a different concept from that of the present invention, since its technique is based on the ratio between the wire area and the area of a doped region and does not suggest the concept of grids from two different circuit design modules. Liu and Finzi both teach interconnecting to a single grid to be protected

to the substrate, an entirely different concept from interconnecting two grids, let alone two circuit design module grids.

2. The Examiner's position fails to provide any "circuit design modules", as this terminology is defined in the specification

As explained in MPEP § 2111, in accordance with the holding in *Philips v/ AWG Corp.*, 415 F.3d 1303, 1313, 75 USPQ2d 1321, 1326 (Fed. Cir. 2005)(*en banc*): "*During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification*." (emphasis by Appellants)

As explained in MPEP §2111.01(I): "*The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation in light of the specification*." (emphasis by Appellants)

As explained in MPEP §2111.01(III): "*It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the "ordinary" and "customary" meaning of the terms in the claims*." (emphasis by Appellants) …. "*The ordinary and customary meaning of a term may be evidenced by a variety of sources, including "the words of the claims themselves, the remainder of the specification, ….*" (emphasis by Appellants)

The present invention is directed to the problem of overvoltage breakdown in SOI devices, not the silicon-based device of primary reference Liu. As explained in paragraph

[0009], the standard model for breakdown in silicon-based devices would suggest that such breakdown should not occur in SOI devices.

However, as explained in paragraph [0010], the present inventors have recognized that the breakdowns that they have noticed in SOI occurs at the boundary of different power or ground networks within the integrated circuit. The inventors subsequently also recognized that the boundary was typically located at two different design modules, as illustrated in Figure 3. The concept of a grid of a circuit design module is described/ defined in paragraph [0034] of the specification, as being the interconnecting grid (typically metal) to relatively large number of points in each of the design portions, and would typically involve either a ground grid or a power grid. None of the three references of record suggest this concept of circuit design module grids or the possibility of a problem related to this concept.

In contrast, Liu is not concerned with the breakdown in an SOI device and is not concerned with preventing accumulated charges between two grids in two different design portions of the circuit.

As clearly shown in Figure 2 of Liu, the breakdown protection 20 is interconnected between the connector 13 and the substrate (see lines 14-15 of column 2 and lines 26-28 of column 3), not between two different grids as required by the claimed invention.

There is no evidence in Liu of different "circuit design modules", let alone any suggestion to interconnect two such circuit design modules to preclude a differential voltage buildup during plasma processing. Nor is there any need in the bulk silicon environment of Liu or Finzi to be concerned with two different "circuit design modules",

since the breakdown mechanism in bulk silicon devices involve a path to the substrate. Without an equivalent concept in Liu that corresponds to the concept of a grid in a circuit design module, Liu fails to satisfy the plain meaning of the claim language of the independent claims and the claimed invention is certainly not obvious in view of the two different breakdown mechanisms and the solution of the present invention to interconnect two circuit design module grids by a protection mechanism.

It is also noted that, to one having ordinary skill in the art, these design module grids would be apparent, since they consist of a relatively large network of (typically metal) connections on the same layer. That is, metallization on the same layer is readily apparent to a viewer and metallization on the same layer that interconnects a large number of points in the circuit would be even more apparent. As such, these grids provide a structure within the integrated circuit that would be readily recognized by one of ordinary skill in the art, either from viewing an actual device or from viewing a schematic of the circuit.

3. The Examiner's position ignores the structure inherent in the claim language

Taking independent claim 19 as an example, the independent claims refer to a "metallization layer", which is clearly a structure within the integrated circuit. This layer is described in the claims as significant because the claimed device also includes a protective means that electrically interconnects the first and second grids, which are also structure within the integrated circuit.

Even if the Examiner chooses to ignore the terminology "that accumulates a charge during a plasma process", the Examiner still has the initial burden of demonstrating two design module grids that are electrically interconnected, as well as pointing out a "metallization layer." As mentioned above, the protective device 20 shown in Figure 2 of Liu interconnects between conductor 13 and the substrate, not between two grids, as required to satisfy the plain meaning of the claim language of the independent claims.

Therefore, even ignoring the "process-oriented" description, the Examiner would still have to locate a metallization layer and two design module grids (as defined in the specification), and a protective device interconnecting these two design module grids.

Even ignoring the specialized "grids" as being "circuit design module" grids, the Examiner would still have to at least demonstrate two different grids. At most, Liu and Finzi's protective devices involve only one grid and the interconnection is to the substrate, not to a second grid.

The rejection of record clearly fails to demonstrate a protective device provided between two grids, let alone two circuit design module grids. As pointed out above, design module grids are structures within the integrated circuit having the specific meaning

described in the specification and would not be satisfied by merely pointing out an arbitrary connection point within a circuit.

4A. The Examiner's position ignores the difference between the silicon-based technology of primary reference Liu and the SOI environment of the present invention

In paragraphs [0004] and [0005] and Figure 1 of the present application, the breakdown in bulk silicon devices is explained, as involving a breakdown mechanism that requires carriers to dissipate to the substrate. This is the breakdown mechanism of Liu and of Finzi.

In contrast, as shown in Figure 2 and explained beginning in paragraph [0030], the present invention involves a breakdown mechanism in an SOI device, wherein the components are isolated from the substrate by the underlying oxide layer BOX. The breakdown in this SOI environment is between two design module grids, not between one grid and the substrate, as in Liu.

4B. The Examiner's position attempts to convert the primary reference into the SOI environment that has a different breakdown mechanism

Since primary reference Liu involves a bulk silicon environment having a breakdown mechanism involving the substrate, converting Liu into the SOI environment, as the Examiner attempts to do with secondary reference Kimura, inherently changes the principle of operation of the breakdown mechanism of the bulk silicon device of Liu. Such change in principle of operation is improper under the holding in *In re Ratti...*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), as described in MPEP §2143.01: "*If the proposed*

modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious."

It is noted that secondary reference Finzi is also a bulk silicon device and does not satisfy the claim language that two grids be interconnected for protection, contrary to the characterization in the rejection of record. That is, Figures 2 and 3 of Finzi clearly shows protective device 220 as connected to the substrate, not between two grids, let alone two grids in two different design modules.

Moreover, in order to modify Liu to interconnect two grids (rather than one grid interconnect to the substrate), the new interconnection between the two grids would interrupt the mechanism of the breakdown in Liu, since the bulk silicon breakdown involves a path to the substrate. Therefore, such modification to change the protection interconnection to be between two grids would defeat the purpose of primary reference Liu. Such modification would be improper under *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984), as described in MPEP §2143.01: "*If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.*"

5. Because of the different breakdown mechanisms, the protective mechanism in primary reference Liu (and secondary reference Finzi) fails to satisfy the plain meaning of the claim language of even the independent claims

Moreover, as explained in the preceding paragraph, primary reference Liu cannot even be modified to satisfy the claimed invention description without changing the principle of operation of the breakdown mechanism in Liu and without defeating the purpose of Liu.

CONCLUSION

In view of the foregoing, Appellants submit that claims 1-10, 19, and 20, all the claims presently pending in the application, are clearly patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove all rejections of claims 1-10, 19, and 20.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 09-0456.

Respectfully submitted,

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Frederick E. Cooperrider
Reg. No. 36,769

McGinn Intellectual Property Law Group, PLLC
8231 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer Number: 21254